In the Claims

51. A method of forming a plurality of DRAM capacitors comprising:

etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps.

52. The method of claim 51 wherein the forming electrically insulative partitions step comprises:

forming insulative material over the substrate; and

conducting an anisotropic etch of the insulative material to a degree sufficient to leave the partitions.

Cancel claim 53.

New Claims

54. The method of claim 51, wherein forming electrically insulative partitions comprises depositing a dielectric layer.

55. The method of claim 51, wherein etching capacitor container openings comprises:

anisotropically etching first capacitor container openings in a first etching step; and

anisotropically etching second capacitor container openings in a second etching step.

56. The method of claim 51, wherein etching capacitor container openings comprises:

anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings.

57. A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate.

58. The method of claim 57, wherein the second capacitor container openings are intercalated between the first capacitor container openings.

59. The method of claim 57, wherein the second capacitor container openings are intercalated between the first capacitor container openings, the method further comprising forming electrically insulative partitions between adjacent capacitors intermediate etching the first and second capacitor container openings.

60. A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings in a first dielectric layer;

forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions.

61. A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings in a first dielectric layer;

forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer;

conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave the partitions after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer.

62. A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings in a first dielectric layer;

forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions.

63. The method of claim 62, wherein forming electrically insulative partitions comprises:

depositing a second dielectric layer; and

conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave the partitions.

64. The method of claim 62 wherein the first dielectric layer comprises silicon dioxide.

65. The method of claim 62 wherein the first dielectric layer comprises borophosphosilicate glass.